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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/734,312	12/15/2003	Naoki Makita	70404.12	1687

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EXAMINER	
RICHARDS, N DREW	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 12/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/734,312	MAKITA, NAOKI	
	Examiner	Art Unit	
	N. Drew Richards	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16,18-20,22-37 and 55-59* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *2,3,5,7,9,11,13,18-20,23,26,27,30,31,35-37,57 and 58* is/are allowed.

6)☒ Claim(s) *1,4,6,8,10,12,14-16,22,24,25,28,29,32-34,55,56 and 59* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/22/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 9/18/06 has been entered.

Election/Restrictions

2. Applicant's election without traverse of Group I, claims 1-3 and 55-58, in the reply filed on 7/20/05 is acknowledged.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claim 59 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 59 includes new matter that is not

supported by the originally filed specification. Claim 59 recites "the gate electrode has side surface inclination angles that change within a range according to the height of the gate electrode" and "the range of the side surface inclination angles of the gate electrode is larger than an inclination angle of the protruding portion of the semiconductor layer." The originally filed specification does not provide support for plural inclination angles in the gate electrode that change according to the height of the gate electrode. The originally filed specification, as shown in figure 1G for example, only provides support for a single inclination angle of the gate electrode and provides no support for different angles simultaneously.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 4, 6, 8, 10, 14-16, 22, 28, 29, 55 and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi (US 2002/0102823 A1) in view of Murakami et al. (US 2002/0068388 A1).

Yamaguchi et al. teach in figure 4 a semiconductor device comprising a thin film transistor including a semiconductor layer 9 (labeled in figures 2 and 3, unlabeled in figure 4) that includes a channel region 13 (on left side), a source region and a drain region 14, a gate insulating film 5 provided on the semiconductor layer, and a gate

electrode 6 for controlling a conductivity of the channel region, wherein a surface of the semiconductor layer includes a protruding portion, and a side inclination angle of the gate electrode is larger than an inclination angle of the protruding portion of the semiconductor layer. As shown, the gate electrode has a side inclination angle of approximately 90 degrees.

Yamaguchi et al. further teaches a cross-section of the gate electrode including first and second opposing sides that are parallel to each other (top and bottom sides) but does not teach a third side that is not parallel to any other side of the cross-section of the gate electrode or the gate electrode having an inclined side surface

Murakami et al. teach in figures 4b and 4c, as well as in finished product 6c, a thin film transistor that includes a channel region, source region, drain region, gate insulating film, and a gate electrode (labeled 310b in figure 4b and 315b in figure 4c) Murakami et al. teach the gate electrode 315b having a cross-section including first and second opposing sides that are parallel to each other (top and bottom sides) and a third side that is not parallel to any other side of the cross-section of the gate electrode (left or right side of the tapered gate) which constitutes an inclined side surface. Murakami et al. teach throughout figures 4b-5a and in paragraphs [0106] and [0112]-[0115] that the tapered gate electrode is used in an implantation process to form LDD regions.

Yamaguchi et al. and Murakami et al. are from the same field of endeavor. At the time of the invention it would have been obvious to one of ordinary skill in the art to employ the tapered gate implantation process of Murakami et al. in the device of Yamaguchi et al. The motivation for doing so is to simultaneously provide regions with

different doping concentrations (such as 401 and 403 of Murakami et al.) to form LDD regions that are effective in reducing the OFF current value of the transistor. In combination, using the tapered gate of Murakami in the device of Yamaguchi et al. the protruding portion would be located under the inclined side surface of the gate electrode. Thus, the combination of Yamaguchi et al. and Murakami et al. teach the invention of claim 1.

With regard to claim 4, as seen in figure 4 Yamaguchi et al. teach multiple protruding portions all having approximately the same side surface inclination angle less than that of the gate.

With regard to claim 6, the side surface inclination angle of the gate is about 75 to 90 degrees. Further, in the combination using the gate and implantation process of Murakami et al., the gate as taught by Murakami et al. has an inclination angle (taper angle) of nearly 90 degrees (see Murakami et al. paragraph [0114]).

With regard to claim 8, an inclination angle of the protruding portion is about 30 to about 70 degrees.

With regard to claim 10, as taught in paragraph [0076] an average height of the protruding portion is about 8 to about 60 nm.

With regard to claim 14, the semiconductor film is a crystalline film and the protruding portions are located over crystal grain boundaries.

With regard to claim 15, as can be seen in figures 3 and 4, the crystal grain boundary is a multipoint where three of more crystal grains meet.

With regard to claim 16, the diameter of the crystal grains is about 100 to about 1000 nm.

With regard to claim 22, the semiconductor layer is a crystalline layer having protrusions formed through a melting/solidification process.

With regard to claims 28 and 29, the semiconductor layer is made up primarily of regions oriented along <111> crystal zone planes wherein 50% or more of the regions are oriented along a (110) plane.

With regard to claims 55 and 56, Yamaguchi et al. teach an electronic device comprising the device of claim 1 and further teach a display section where an image is displayed by using the semiconductor device (see figure 5).

7. Claims 1, 4, 6, 8, 10, 14-16, 22, 28, 29, 55 and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue et al. (US Patent No. 5,693,959) in view of Murakami et al. (US 2002/0068388 A1).

Inoue et al. teach in figure 1, for example, a thin film transistors as claimed in claim 1. Inoue et al. teach a semiconductor layer having protruding portions (under contacts 106a/106b) where a side inclination angle of the gate 104 is greater than an inclination angle of the protruding portions.

Inoue et al. further teaches a cross-section of the gate electrode including first and second opposing sides that are parallel to each other (top and bottom sides) but does not teach a third side that is not parallel to any other side of the cross-section of the gate electrode or the gate electrode having an inclined side surface.

Murakami et al. teach in figures 4b and 4c, as well as in finished product 6c, a thin film transistor that includes a channel region, source region, drain region, gate insulating film, and a gate electrode (labeled 310b in figure 4b and 315b in figure 4c) Murakami et al. teach the gate electrode 315b having a cross-section including first and second opposing sides that are parallel to each other (top and bottom sides) and a third side that is not parallel to any other side of the cross-section of the gate electrode (left or right side of the tapered gate) which constitutes an inclined side surface. Murakami et al. teach throughout figures 4b-5a and in paragraphs [0106] and [0112]-[0115] that the tapered gate electrode is used in an implantation process to form LDD regions.

Inoue et al. and Murakami et al. are from the same field of endeavor. At the time of the invention it would have been obvious to one of ordinary skill in the art to employ the tapered gate implantation process of Murakami et al. in the device of Inoue et al. The motivation for doing so is to simultaneously provide regions with different doping concentrations (such as 401 and 403 of Murakami et al.) to form LDD regions that are effective in reducing the OFF current value of the transistor. In combination, using the tapered gate of Murakami in the device of Inoue et al. the protruding portion would be located under the inclined side surface of the gate electrode. Thus, the combination of Inoue et al. and Murakami et al. teach the invention of claim 1.

With regard to claim 4, Inoue et al. teach multiple protruding portions all having approximately the same side surface inclination angle less than that of the gate.

With regard to claim 6, the side surface inclination angle of the gate is about 75 to 90 degrees. Further, in the combination using the gate and implantation process of Murakami et al., the gate as taught by Murakami et al. has an inclination angle (taper angle) of nearly 90 degrees (see Murakami et al. paragraph [0114]).

With regard to claim 8, an inclination angle of the protruding portion is about 30 to about 70 degrees.

With regard to claim 10, as taught in column 6 lines 46-48 an average height of the protruding portion is about 8 to about 60 nm.

With regard to claim 22, the semiconductor layer is a crystalline layer having protrusions formed through a melting/solidification process.

With regard to claim 34, Inoue et al. teach a lightly-doped impurity region 102b/102f at a junction between the channel and the source or drain region.

With regard to claims 55 and 56, Inoue et al. teach an electronic device comprising the device of claim 1 and further teach a display section where an image is displayed by using the semiconductor device (see figures 7 or 8 for example).

8. Claims 1, 4, 6, 8, 10, 14-16, 22, 28, 29, 55 and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi et al. (US 2003/0080384 A1) in view of Murakami et al. (US 2002/0068388 A1).

Takahashi et al. teach in figure 5(c) a semiconductor device including a thin film transistor including a semiconductor layer 71 that has a protruding portion, an insulator

69, a gate 70, a source and drain 66, where an inclination angle of the gate is greater than an inclination angle of the protruding portion.

Takahashi et al. further teaches a cross-section of the gate electrode including first and second opposing sides that are parallel to each other (top and bottom sides) but does not teach a third side that is not parallel to any other side of the cross-section of the gate electrode and the gate electrode having an inclined side surface.

Murakami et al. teach in figures 4b and 4c, as well as in finished product 6c, a thin film transistor that includes a channel region, source region, drain region, gate insulating film, and a gate electrode (labeled 310b in figure 4b and 315b in figure 4c) Murakami et al. teach the gate electrode 315b having a cross-section including first and second opposing sides that are parallel to each other (top and bottom sides) and a third side that is not parallel to any other side of the cross-section of the gate electrode (left or right side of the tapered gate) which constitutes an inclined side surface. Murakami et al. teach throughout figures 4b-5a and in paragraphs [0106] and [0112]-[0115] that the tapered gate electrode is used in an implantation process to form LDD regions.

Takahashi et al. and Murakami et al. are from the same field of endeavor. At the time of the invention it would have been obvious to one of ordinary skill in the art to employ the tapered gate implantation process of Murakami et al. in the device of Takahashi et al. The motivation for doing so is to simultaneously provide regions with different doping concentrations (such as 401 and 403 of Murakami et al.) to form LDD regions that are effective in reducing the OFF current value of the transistor. In combination, using the tapered gate of Murakami in the device of Takahashi et al. the

protruding portion would be located under the inclined side surface of the gate electrode. Thus, the combination of Takahashi et al. and Murakami et al. teach the invention of claim 1.

With regard to claim 4, Takahashi et al. teach multiple protruding portions all having approximately the same side surface inclination angle less than that of the gate.

With regard to claim 6, the side surface inclination angle of the gate is about 75 to 90 degrees. Further, in the combination using the gate and implantation process of Murakami et al., the gate as taught by Murakami et al. has an inclination angle (taper angle) of nearly 90 degrees (see Murakami et al. paragraph [0114]).

With regard to claim 12, an average surface roughness of the surface of the semiconductor layer is about 4 to about 30 nm.

With regard to claim 55, Takahashi et al. teach an electronic device comprising the device of claim 1.

9. Claims 24, 25 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi et al. with Murakami et al. as applied to claims 1, 4, 6, 8, 10, 14-16, 22, 28, 29, 55 and 56 above, and further in view of Yamazaki et al. (US 2002/0100937 A1).

Yamaguchi et al. teach forming their layer using a melting/solidification process but do not teach including a catalyst element capable of promoting crystallization of an amorphous semiconductor film.

Yamazaki et al. teach adding a catalyst element to a semiconductor film to promote crystallization during a melting/solidification process.

At the time of the invention it would have been obvious to one of ordinary skill in the art to include a catalyst element in the semiconductor layer of Yamaguchi in order to promote crystallization to form a crystalline layer having excellent crystallinity.

With regard to claim 25, Yamazaki teach that the catalyst element is nickel (Ni).

With regard to claim 32, Yamaguchi et al. teaches the crystal grains having the same diameter as in the instant invention (about 100nm to about 1000nm as recited in claim 16 above) but is silent as to a "domain diameter of crystal domains." Nonetheless, the claimed range of about 2 micron to about 10 micron is considered obvious over Yamaguchi et al. in view of Yamazaki et al. It is obvious that when the catalyst element of Yamazaki et al. is incorporated into the melting/solidification process of Yamaguchi et al. the resulting domain diameters of the semiconductor film will have the claimed diameter. As explained in paragraph [0106] of applicant's specification, when a catalyst is used (during the crystallization process) the domain diameters are typically about 2 micron to about 10 micron. Thus, applicant's specification provides evidence that when the catalyst is used the claimed domain diameter will result. Thus, even though Yamaguchi et al. and Yamazaki et al. do not explicitly teach a domain diameter, the device resulting from their combination will have the claimed domain diameter.

Allowable Subject Matter

10. Claims 2, 3, 5, 7, 9, 11, 13, 18-20, 23, 26, 27, 30, 31, 35, 36, 37, 57 and 58 are allowed.

11. The following is an examiner's statement of reasons for allowance: Prior art of record fails to teach, disclose, or suggest, either alone or in combination, the device as recited in claim 2 including a gate electrode includes a first step portion and a second step portion provided on the first step portion, and a side surface inclination angle of each of the first and second step portions is larger than an inclination angle of the protruding portion of the semiconductor layer.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

12. Applicant's arguments filed 9/18/06 have been fully considered but they are not persuasive.

Applicant has argued that the Examiner has failed to provide proper motivation for modifying each of the references to have the tapered gate electrode of Murakami et al. because the tapered gate is not necessary in the formation of the LDD regions. Initially, it is noted that applicant has not provided any reasoning or evidence as to why

the tapered gate is alleged to not be necessary in the formation of the LDD regions. Applicant furthers this argument by stating that the Examiner has failed to explain why it would be necessary to use tapered gate electrodes to provide the LDD regions. This argument is not persuasive. In establishing a case of *prima facie* obviousness, it is not incumbent upon the Office to prove why using the particular technique taught by the reference is necessary, but merely to prove that using the particular technique is obvious and desirable to one of ordinary skill in the art. In this case, the Office has provided clear reasoning for the motivation as explicitly stated in the reference itself. Murakami et al. teach that the tapered gate is a desirable technique for forming LDD regions such that the OFF current value can be reduced. The fact that other techniques may exist in the art does not change the fact that the particular technique of Murakami et al. is obvious.

Applicant also argues that each of Yamaguchi, Inoue et al. and Takahashi et al. fail to teach a gate having an inclined surface and thus the protruding portion located under the inclined side surface of the gate. This is not persuasive as this argument merely argues against the references individually when the claim has been rejected over a combination. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Applicant also argues that Murakami et al. does not teach the surface of the semiconductor layer has a protruding portion and the protruding portion being located under the inclined side surface of the gate. This is not persuasive as this argument merely argues against the references individually when the claim has been rejected over a combination. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Applicant also argues that neither Murakami et al. nor any other prior art reference of record provides motivation or suggestion to modify Yamaguchi, Inoue et al. or Takahashi et al. such that the protruding portion is located under the inclined surface of the gate electrode. This is not persuasive as in combining Murakami et al.'s tapered gate into the devices of Yamaguchi, Inoue et al. or Takahashi et al. the "protruding portion is located under the inclined surface of the gate electrode" would be the necessary result. Since the gate is taught in all references applied as being formed above the semiconductor layer (in which the protruding portion exists) the protruding portion in always taught as being underneath the gate. Modifying the gate to include inclined side surfaces will still necessarily have the protruding portions below the gate and thus under the inclined side surfaces. Restated, this limitation is a necessary result of the combination and does not require adapting of modifying the references any more than already done in including the tapered gate.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (571) 272-1736. The examiner can normally be reached on Monday-Friday 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

N. DREW RICHARDS
PRIMARY EXAMINER